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10/538,371	06/13/2005	Santanu Dutta	US02 0563 US	6034

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EXAMINER	
PARIKH, KALPIT	
ART UNIT	**PAPER NUMBER**
2187	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/538,371	DUTTA, SANTANU	
	Examiner	Art Unit	
	Kalpit Parikh	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *13 June 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. APPLICATION INFORMATION

The instant application having Application No. 10538371 has a total of 16 claims pending in the application; there are 3 independent claim and 13 dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by M.P.E.P. ' 201.14(c), acknowledgment is made of applicant's claim for priority based on a 371 of PCT/IB03/05797 filed on December 9, 2003 which claims priority to U.S. provisional application 60/432,756 filed December 12, 2002.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by M.P.E.P. ' 609 (C), the applicant's submission of the Information Disclosure Statement dated June 13, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. ' 609 C(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. REJECTIONS NOT BASED ON PRIOR ART

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because the description of the drawings in the specification does not appear to correspond to the submitted drawings. The description of the drawings appears to correspond to the drawings submitted in the U.S. provisional application 60/432,756. Clarification is respectfully requested.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **CLAIMS 1,4 AND 7** rejected under 35 U.S.C. 102(b) as being anticipated by Rickard et al. (US Pat No. 6041397)

   As per claim 1 and 7, Rickard et al. disclose a buffer management system, comprising:

   - a buffer memory (see COL 1 LINE 25), and
   - a controller , operably coupled to the buffer memory, that is configured to
     - o partition the buffer memory into a plurality of independent buffers, dependent upon a partition parameter (see COL 1 LINE 36: 'blocking factor') that determines a quantity of the plurality (see COL 1 LINES 34-36)

[Rickard et al. disclose the partitioning the memory into a plurality buffers based on a blocking factor.]

- o wherein each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two, to facilitate circular-access to the buffer (see COL 1 LINES 36-37)

  [Rickard et al. teach facilitating circular-access to the buffer because Rickard et al. teach the buffer size is a power of two.]

As per claim 4, the buffer management system of claim 1, wherein the controller is further configured to

- allocate the plurality of independent buffers among a plurality of source-destination paths (see FIG 1-2)

  [The buffers are allocated for transmission of data from the planarity of source nodes to the plurality of destination nodes (see COL1 LINES 59-65).]

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **CLAIMS 1-3 AND 5-11** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309).

As per claim 1 and 7, Shemla et al. disclose a buffer management system, comprising:

- a buffer memory (see Shemla et al. FIG 1: 12), and
- a controller , operably coupled to the buffer memory, that is configured to (see Shemla et al. FIG 1: 10)
    - o partition the buffer memory into a plurality of independent buffers (see Shemla et al. FIG 2: 40),
    - o wherein each buffer of the plurality of independent buffers has a buffer-size that is an integer power of two, to facilitate circular-access to the buffer (see Shemla et al. FIG 2: 'FIFO 0')

      [Shemla et al. teach facilitating circular-access to the buffer because Shemla et al. teach the buffer size is a power of two.]

However, Shemla et al. do not expressly disclose the partitioning is

- dependent upon a partition parameter that determines a quantity of the plurality

In the same field of endeavor, Brown et al. disclose partitioning a memory into a plurality of buffers

- dependent upon a partition parameter that determines a quantity of the plurality (see Brown et al. ABSTRACT)

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to partition a buffer based on a partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claim 2, and 9, Shemla et al. disclose the buffer management system of claim 1, wherein

- the controller is configured to include a circular-increment function that requires only an address-increment function (see Shemla et al. COL 3 LINES 44-46) and a bit-overwrite function to effect a circular-increment of a pointer to a select buffer of the plurality of independent buffers (see Shemla et al. COL 3 LINES 44-46 AND LINES 48-51)

  [Shemla et al. disclose a circular buffer because Shemla et al. disclose the pointers are incremented to access a next buffer location.]

As per claim 3 and 8, Shemla et al. disclose the buffer management system of claim 1,

- wherein the buffer-sizes of the plurality of independent buffers are equal (see Shemla et al. FIG 2)

As per claim 5 and 10, Shemla et al. disclose the buffer management system of claim 1, wherein

- the controller is further configured to provide a write-interface and a read-interface to one or more applications (see Shemla et al. FIG 1: 14 AND 16),
  - o the write-interface requiring only an identification of data to be stored (see FIG 1: 'DATA IN') and an identification of a select buffer of the plurality of independent buffers to store the data (see FIG 1: 'FIFO_WR_REQ'), and
  - o the read-interface requiring only the identification of the selected buffer (see FIG 1: 'FIFO_RD')

As per claims 6 and 11, Shemla et al. disclose the buffer management system of claim 1, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and
- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

6. **CLAIMS 12-13 AND 15-16** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309).

As per claim 12, Shemla et al. disclose an integrated circuit, comprising

- a buffer memory (see Shemla et al. FIG 1: 12), and
- a controller (see Shemla et al. FIG 1: 10) that includes write control logic (see Shemla et al. FIG 1: 14 AND 22), and read control logic (see Shemla et al. FIG 1: 16 AND 24), wherein the controller is configured to

- o partition the buffer memory into a plurality of buffers (see Shemla et al. FIG 2: 40), each buffer of the plurality of buffers having a size that is an integer power of two (see Shemla et al. FIG 1: 'FIFO 0'), and
- o the write control logic and read control logic are each configured to facilitate use of each buffer as a circular buffer (see Shemla et al. COL 3 LINES 48-51)

  [Shemla et al. disclose the pointer values are incremented by one after each read or write. Incrementing in such a manner is construed to facilitate the use of each buffer as a circular buffer.]

However, Shemla et al. do not expressly disclose the partitioning of the buffer memory may be

- based on a partition parameter that is provided to the controller

  [Shemla et al. disclose partitioning the buffer into N partitions, however Shemla et al. do not expressly disclose the partitioning is based on a partition parameter provided to the controller.]

In the same field of endeavor, Brown et al. disclose partitioning a buffer

- based on a partition parameter that is provided to the controller (see Brown et al. COL 3 LINE 39-45: 'communication parameter')

Brown et al. and Shemla et al. are analogous art because they are from the same field of endeavor, namely memory access and control.

At the time of invention it would have bee obvious to a person of ordinary skill in the art to modify the circuit of Shemla et al. to partition a buffer based on a

partition parameter provided to the controller as suggested by Brown et al. (see Brown et al. COL 3 LINES 39-45).

The suggestion/motivation for doing so would have been because Brown et al. disclose the method of dynamically partitioning the memory based on a parameter improves memory utilization (see Brown et al. COL 5 LINES 28-37).

Therefore it would have been obvious at the time of invention to modify the circuit of Shemla et al. to partition the memory based on a partitioning parameter as taught by Brown et al. for the benefit of improved memory utilization to arrive at the invention as specified in the claims.

As per claim 13 Shemla et al. disclose the integrated circuit of claim 12, wherein

- the sizes of the plurality of buffers are equal (see Shemla et al. FIG 3).

  [Shemla et al. disclose the partitioning of the memory into a plurality of equal size buffers.]

As per claim 15, Shemla et al. disclose the integrated circuit of claim 1, wherein

- the write control logic effects a storage of a data value to a select buffer of the plurality of buffers based only on an identification of the data value and an identification of the select buffer (Shemla et al. COL 3 LINES 27-45), and

  [Shemla et al. disclose the circuit performs a write by selecting a buffer based on the identification of the selected buffer.]

- the read control logic effects a retrieval of the data value based only on the identification of the select buffer (see Shemla et al. COL 3 LINES 52-65)

  [Shemla et al. disclose the circuit performs a read based on the identification of the select buffer.]

As per claim 16, Shemla et al. disclose the buffer management system of claim 1, wherein

- the buffer memory is addressed by an M-bit address (see Shemla et al. COL 3 LINE 20: 'WR_ADDR') each buffer of the plurality of independent buffers is indexed by an N-bit index (see Shemla et al. COL 3 LINE 25: 'WR_SEL') that forms a set of N most-significant-bits of the M-bit address (see Shemla et al. COL 3 LINES 25-26: 'upper 3 bits'), and
- the size of each buffer is at least 2^{M-N} (see Shemla et al. FIG 2: 40)

7. **CLAIM 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Shemla et al. (US Pat No. 5809557) in view of Brown et al. (US Pat No. 5916309) as applied to claim 12 above, and further in view of Fadivi-Ardekani et al. (US Pat No. 6496916).

As per claim 14, Shemla et al. the integrated circuit of claim 12, wherein

- the use of each buffer as a circular buffer requires circular-addressing, and the controller is configured to effect the circular-addressing via an incrementer that is configured to increment an address to the buffer memory (see Shemla et al. COL 3 LINES 46-51), and

However, Shemla et al. do not expressly disclose

- a bit masker that is configured to overwrite select bits of the address, corresponding to an index to the buffer within the buffer memory

[Shemla et al. disclose the upper bits of the write address are utilized as the index into the buffer, however Shemla et al. do not disclose masking the upper bits of the write address.]

In the same field of endeavor Fadivi-Ardekani et al. disclose a memory partitioning circuit wherein

- a bit masker that is configured to overwrite select bits of the address (i.e., the upper bits), corresponding to an index to the buffer within the buffer memory (see Fadivi-Ardekani et al. FIG 2 AND FIG 3).

Fadivi-Ardekani et al. and Shemla et al. are analogous art because they are from the same field of endeavor namely, memory partitioning.

At the time of invention it would have been obvious to a person of ordinary skill in the art to modify the addressing of Shemla et al. write mask the index bits (i.e., 'WR_SEL' bits) of the WR_ADDR as suggested by Fadivi-Ardekani et al. (see Fadivi-Ardekani et al. FIG 2 AND COL 2 LINES 18-24).

The suggestion/motivation for doing so would have been because Fadivi-Ardekani et al. disclose the masking of the upper bits to address a partitioned memory improves memory access timing (see Fadivi-Ardekani et al. COL 2 LINES12-15).

Therefore it would have been obvious at the time of invention to modify addressing mechanism of Shemla et al. to mask the index bits of Shemla et al. as suggested by Fadivi-Ardekani et al. for the benefit of improved access timing to arrive at the invention as specified in the claims.

IV. CLOSING COMMENTS

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

The following references teach adapting a size of a buffer of a communication system.

U.S. PATENT NUMBER	RELEVANT PORTIONS
5974518	ABSTRACT AND FIG 2

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

IVa. CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-16 have received a first action on the merits and are subject of a first action non-final.

For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

V. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kalpit Parikh whose telephone number is (571) 270-1173. The examiner can normally be reached on MON THROUGH FRI 7:30 TO 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kalpit Parikh/

May 9, 2007

Kalpit Parikh
Examiner
Art Unit 2187

DONALD SPARKS
SUPERVISORY PATENT EXAMINER